A K-Band Monolithic Oscillator Integrated with a Buffer Amplifier Using a Device-Circuit Interaction Design Concept

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Abstract— **We report on a high power, high efficiency, and small-size monolithic coplanar waveguide oscillator incorporating a single-stage buffer amplifier on the same chip. For the oscillator design, by changing RF current level through the device, the optimum load line was chosen in order to have an oscillation frequency insensitive to the effect of the subsequently connected amplifier, based on a device-circuit interaction concept. The amplifier, on the other hand, which was driven directly by the oscillator, was designed to achieve an overall high power and high efficiency operation. At 21 GHz, the output power of the developed chip recorded 17 dBm with an overall dc-RF efficiency of 22%. By changing the length of a source feedback line, the oscillation frequency was varied from 21 GHz to 26 GHz. For all cases, the output power remained higher than 16 dBm.**

I. Introduction

INCREASING demand for K- and V-band wireless communications systems [1], [2] has stimulated development of small-size local oscillators operating at these frequency bands with a sufficiently high output power to drive RX/TX modules in a transceiver. Heterojunction FET (HJFET) technology permits integration of all transceiver elements on the same chip and, thus, promises overall system chip size reduction. Since the output power level of an oscillator is limited [3]–[6] and decreases with increasing frequency, it is advantageous to integrate a buffer amplifier with the oscillator to enhance the output power. Application of a buffer amplifier will also help to improve the overall dc-RF efficiency and frequency-pulling characteristics of the oscillator.

Recently reported attempts to develop a monolithic oscillator incorporating a buffer amplifier on the same chip include an 11 GHz MESFET oscillator with 17 dBm output power and 20% efficiency [7], and a Q-band MESFET VCO with 19.7 dBm and 7% efficiency [8]. To fulfill the requirement for K-band wireless systems, the present paper describes a small-size high power high efficiency K-band MMIC oscillator by incorporating a single-stage buffer amplifier on the same chip, which provides 17 dBm output power with 22% efficiency.

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II. Circuit Design

A. Oscillator

In the case of a buffer amplifier driven by an oscillator, oscillation frequency fluctuation by an impedance change of an external load will be greatly suppressed due to an inherent amplifier output-input isolation. For further suppression of the frequency fluctuation, a multistage amplifier is employed. To obtain a small-size chip with high efficiency characteristics, however, a new approach to oscillator design with a single stage amplifier must be devised. A device-circuit interaction concept has been discussed for the purpose of minimizing oscillator phase noise [9]. In the present paper, the above concept is applied to suppression of the oscillation frequency fluctuation. For the present oscillator design, an inverse locus of oscillator impedance with respect to RF current and a locus of amplifier impedance with respect to frequency are designed to cross at the oscillation point orthogonally.

Recent trends in microwave and millimeter-wave circuit design employ a large-signal device model on a circuit simulator. This approach enables us to know various information that can not be acquired experimentally and helps design satisfying the above mentioned requirement. A simple circuit to generate a negative impedance, Z_{NEG}, is shown in Fig. 1(a). The circuit includes an FET, a capacitor and an inductor to supply dc-bias, and capacitive and inductive lines, T_S, T_G, connected to the source and gate terminals of the FET, respectively. In the large-signal simulation, the Curtice-Cubic model was employed for the FET. The oscillator design employed here is explained as following steps:

1) Injecting RF power from external source at a desired oscillation frequency into the drain port of the FET, causing RF current, I_{RF} [Fig. 1(a)], and measuring Z_{NEG} for various I_{RF} values by changing power level of the external source. Z_{NEG} is calculated from the injected and reflected waves measured by an ideal coupler on a harmonic balance simulator. Initial lengths of T_S and T_G are selected so that $-\mathrm{Re}(Z_{\mathrm{NEG}})$ is maximum at small-signal operation.
2) Choosing I_{RF} values at large-signal operation. In our design, we select three RF currents $\sqrt{|I_{\mathrm{RF}}|^2}$ as 10, 17, and 22 mA. Corresponding load lines, viewed from the

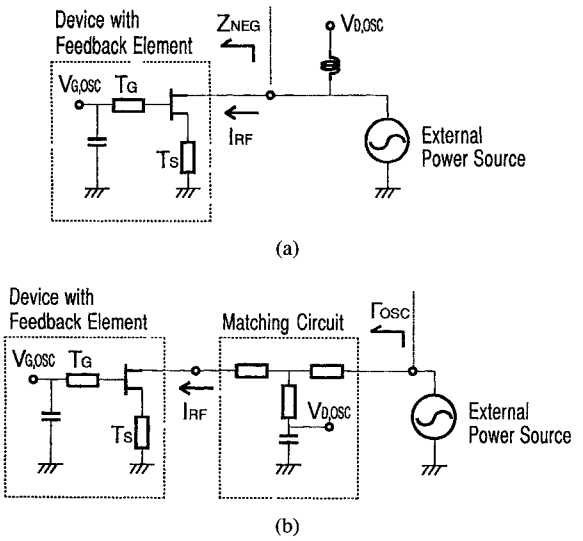

Fig. 1. Setups (a) for calculating load line, RF current and negative impedance using a harmonic balance simulator, and (b) for calculating oscillator reflection coefficient.

drain port of the FET, are represented by LINE A, LINE B and LINE C in Fig. 2, respectively, when matching loads satisfying the oscillation condition are added.

3) Calculating output power, $P_{\rm OUT}$, according to: $P_{\rm OUT} = -{\rm Re}(Z_{\rm NEG}) \cdot |\overline{I_{\rm RF}}|^2$. For the selected $I_{\rm RF}$ conditions, optimum lengths of T_S and T_G can be found to get the maximum $P_{\rm OUT}$ at the desired frequency.
4) Designing each matching circuit so that its impedance, $Z_{\rm LOAD}$, is equal to $-Z_{\rm NEG}$ for the optimum lengths of T_S and T_G. The matching circuit is designed to transform $Z_{\rm LOAD}$ into a 50 Ω load.
5) Calculating inverse oscillator reflection coefficients ($\Gamma^{-1}_{{\rm OSC},A}, \Gamma^{-1}_{{\rm OSC},B}$ and $\Gamma^{-1}_{{\rm OSC},C}$) in Fig. 1(b), and plotting them versus RF current as shown in Fig. 3. Each $\Gamma^{-1}_{\rm OSC}$ locus intercepts zero point in the Γ-plane at the designed RF current. It is important to note that the locus of $\Gamma^{-1}_{\rm OSC}$ can be changed by varying an intercept angle (θ) through adjusting the load line. In Fig. 3, S_{11} of a buffer amplifier designed later is also traced versus frequency. In the case of LINE A, the loci of $\Gamma^{-1}_{{\rm OSC},A}$ and S_{11} cross nearly orthogonally as is desired ($\theta \sim 90°$). Output power variation among three types is within 1 dB and is acceptable.

B. Buffer Amplifier

The amplifier is designed to be driven directly by the oscillator to achieve an overall high power and high efficiency operation. From the definition, the oscillator dc-RF efficiency, $\eta_{\rm OSC}$, and the overall dc-RF efficiency, $\eta_{\rm ALL}$, have following relationship

$$\eta_{\rm ALL} = \frac{G}{1 + (P_{\rm dc,AMP}/P_{\rm dc,OSC})} \cdot \eta_{\rm OSC}$$

where G is the gain under operation, and $P_{\rm dc,OSC}$ and $P_{\rm dc,AMP}$ are oscillator and amplifier dc power consumption, respectively. To improve efficiency, it is required that $G > (1 + P_{\rm dc,AMP}/P_{\rm dc,OSC})$. This consideration suggests that the amplifier has to have high-gain and low-power-dissipation characteristics.

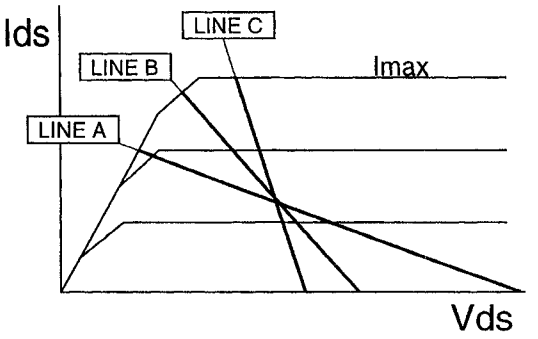

Fig. 2. Load lines, LINE A, LINE B and LINE C for three oscillators designed at RF current of 10, 17, and 22 mA, respectively.

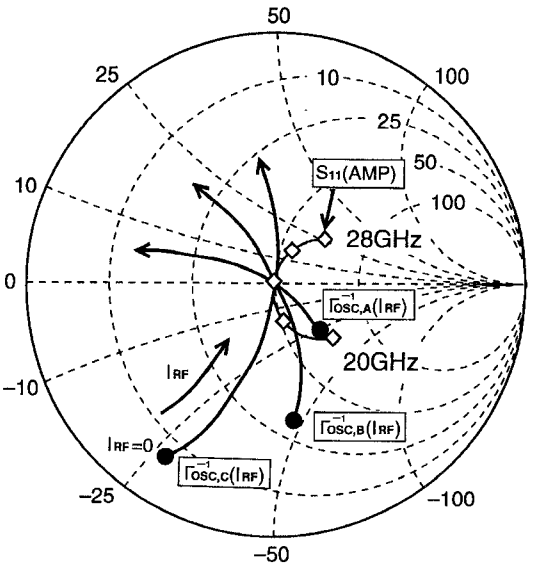

Fig. 3. Calculated inverse oscillator reflection coefficients ($\Gamma^{-1}_{{\rm OSC},A}, \Gamma^{-1}_{{\rm OSC},B}$ and $\Gamma^{-1}_{{\rm OSC},C}$) at 24 GHz with respect to RF current for three load lines, LINE A, LINE B and LINE C, respectively. The locus of S_{11} of a buffer amplifier versus frequency is also demonstrated.

The requirements for the buffer amplifier design are 1) operation at a center frequency of 24 GHz, 2) incorporation of an inductive feedback line in the source terminal of the FET to ensure the stability of the amplifier, and 3) determination of the length of the feedback line to make the amplifier operate near the output saturation point with a high gain (~8 dB). Applying a large-signal harmonic balance method, the circuit parameters were optimized to satisfy the above requirements. Both the input and output ports of the amplifier were designed to be widely matched to a 50 Ω impedance.

An equivalent circuit for the complete *K*-band oscillator with the buffer amplifier is shown in Fig. 4. The devices for both the oscillator and the buffer amplifier are 0.15 μm × 200 μm AlGaAs/InGaAs HJFET's. To realize the feedback line and matching circuit, we use coplanar waveguides (CPW's). The advantages over conventional microstrip lines include simplifying the MMIC process and easy on-wafer probe testing. In order to reduce losses due to the long feedback line of the oscillator and others, we employ relatively wide 50 Ω CPW's (signal line width = 50 μm and

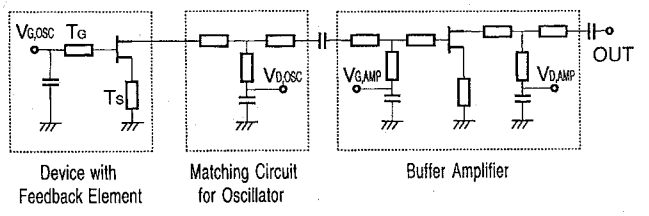

Fig. 4. Equivalent circuit for the K-band monolithic oscillator incorporating a buffer amplifier.

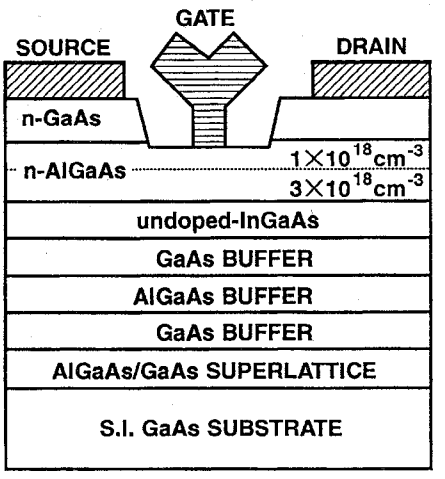

Fig. 5. Cross-sectional view for a step-doped AlGaAs/InGaAs HJFET.

gap = 37 μm). The estimated transmission loss is 0.4 dB per wavelength at 24 GHz.

III. Fabrication Process and Device Characteristics

The K-band oscillator with the buffer amplifier was fabricated on a 3-inch GaAs substrate. A cross-sectional view for an AlGaAs/InGaAs HJFET used in the MMIC is represented in Fig. 5. The epitaxial layer structure consists of an AlGaAs/GaAs superlattice, GaAs and AlGaAs buffers, a 13 nm $In_{0.2}Ga_{0.8}As$ channel, a 40 nm step-doped 1×10^{18} cm^{-3}/3×10^{18} cm^{-3} $Al_{0.2}Ga_{0.8}As$, and an 80 nm n^+-GaAs cap layer. In the FET fabrication process, mesa-isolation, conventional photo-lithography, electron beam evaporation and lift-off techniques have been employed. Details have been reported elsewhere [10] [11]. A metal-insulator-metal (MIM) structure with SiN film as a dielectric layer was applied for fabricating both dc blocking and bypass capacitors. The CPW structure utilizes a 2 μm thick Au-plated layer.

The HJFET has a gate length of 0.15 μm and a total gate width of 200 μm (25 μm × 8). The device has a typical transconductance of 380 mS/mm and an f_T of 70 GHz both at a drain bias of 2 V with a reverse gate-drain breakdown voltage of 11 V. Measured minimum noise figure for the device is 1.1 dB at 24 GHz with an associated gain of 9.5 dB.

IV. Performances

A. Oscillator

Before discussing the overall oscillator-amplifier characteristics, the oscillator performance without a buffer amplifier is demonstrated. Fig. 6 shows a chip photograph for the CPW

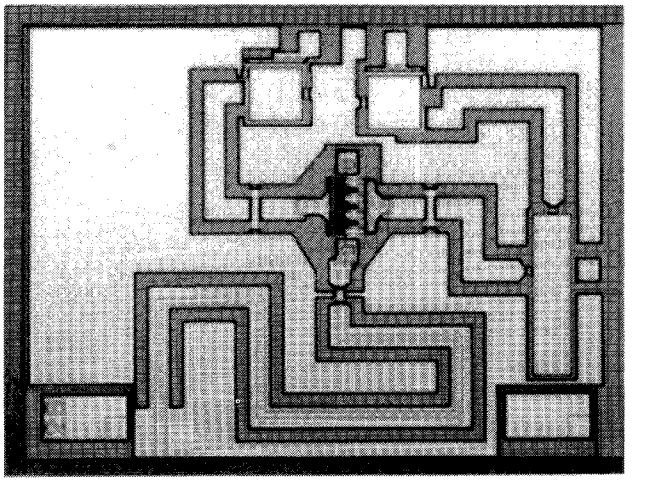

Fig. 6. Chip photograph for the K-band CPW oscillator (1.45 × 1.07 mm^2).

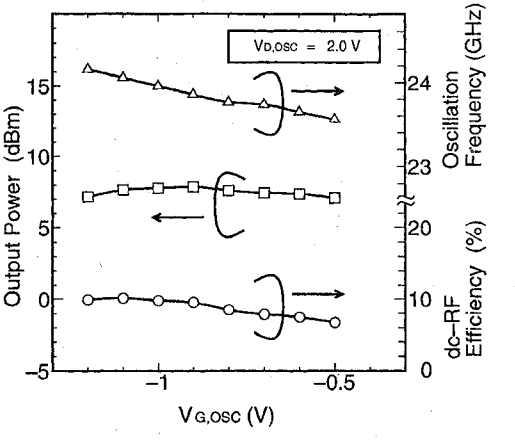

Fig. 7. Oscillator output power, oscillation frequency, and dc-RF efficiency at drain voltage, $V_{D,\mathrm{OSC}} = 2.0$ V, as a function of gate voltage ($V_{G,\mathrm{OSC}}$).

oscillator. The chip size is 1.45 mm × 1.07 mm × 0.26 mm. Fig. 7 depicts output power, oscillation frequency, and dc-RF efficiency at drain voltage, $V_{D,\mathrm{OSC}} = 2.0$ V, as a function of gate voltage, $V_{G,\mathrm{OSC}}$. For $V_{G,\mathrm{OSC}}$ from −1.2 V to −0.5 V, oscillation output power of 7.5 ± 0.4 dBm was observed at around 24 GHz. The oscillation frequency was very close to the designed value of 24 GHz and the output power was about 1 dB lower than the predicted performance. The dc-RF efficiency was 7 ∼ 10% and the oscillator pushing figure was about −800 MHz/V. Fig. 8 indicates output power and dc-RF efficiency as a function of drain voltage, $V_{D,\mathrm{OSC}}$. For a drain voltage of 3 V, the output power was increased to 10.9 dBm while dc-RF efficiency remained almost unchanged.

B. Oscillator Integrated with Buffer Amplifier

A chip photograph for the fabricated K-band CPW oscillator with the buffer amplifier is shown in Fig. 9. The MMIC chip size is 2.22 mm × 1.07 mm × 0.26 mm. Three different oscillators were developed by changing the length of the 50 Ω line, T_S, as 0.43λ, 0.41λ, and 0.38λ, which resulted in oscillation at around 21 GHz, 24 GHz, and 26 GHz, respectively. In the above expressions, λ is the wavelength of each line at 24 GHz. Other circuit parameters of these

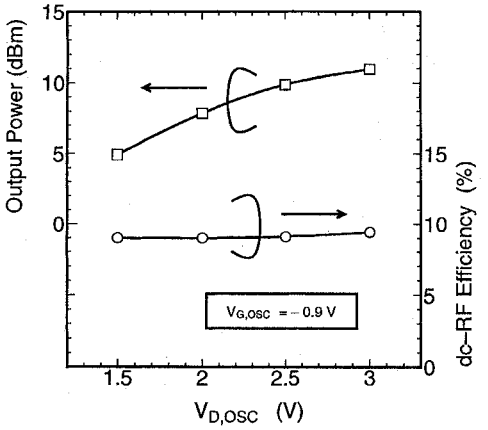

Fig. 8. Output power and dc-RF efficiency as a function of drain voltage ($V_{D,\mathrm{OSC}}$).

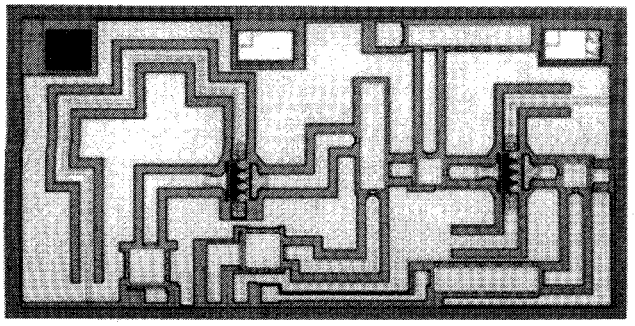

Fig. 9. Chip photograph for the K-band CPW oscillator incorporating a buffer amplifier (2.22×1.07 mm^2).

oscillators were the same, including the length of the 50 Ω line, T_G, as 0.10λ.

Output power, oscillation frequency, and dc-RF efficiency as a function of amplifier drain voltage, $V_{D,\mathrm{AMP}}$, for the case of the 24 GHz oscillator are shown in Fig. 10. For oscillator gate voltage, $V_{G,\mathrm{OSC}} = -0.57$ V, drain voltage, $V_{D,\mathrm{OSC}} = 2.0$ V, and amplifier gate voltage, $V_{G,\mathrm{AMP}} = -0.42$ V, the output power increased with $V_{D,\mathrm{AMP}}$, and reached a maximum value of 14 dBm at $V_{D,\mathrm{AMP}} = 3.0$ V. The overall dc-RF efficiency exhibited its maximum value of 17% at around $V_{D,\mathrm{AMP}} = 2.0$ V. When $V_{D,\mathrm{AMP}}$ was varied from 0.5 V to 3.0 V, resulting in variations of the FET drain-source capacitance connected to an external load through the matching circuit, the oscillation frequency shifted only 160 MHz. On the other hand, for the 21 GHz and 26 GHz oscillators, the oscillation frequencies with respect to $V_{D,\mathrm{AMP}}$ shifted at rates of -380 MHz/V and $+320$ MHz/V, respectively. We believe that these were caused due to intercept angle deviation from 90°, which are calculated to be 20° and 150°, respectively. For the 24 GHz oscillator with a buffer amplifier, the output power was enhanced by 7 dB and the dc-RF efficiency was improved by 10%, compared to the un-buffered oscillator. The oscillator pushing figure was about -90 MHz/V, which is less than that for the unbuffered oscillator.

Fig. 11 represents the maximum output power and overall dc-RF efficiency for each oscillator at $V_{D,\mathrm{OSC}} = V_{D,\mathrm{AMP}} = 2.0$ V and $V_{D,\mathrm{OSC}} = V_{D,\mathrm{AMP}} = 3.0$ V. When the bias voltage was increased from 2 V to 3 V, the output power increased by about 4 dB. For all oscillators, the output power

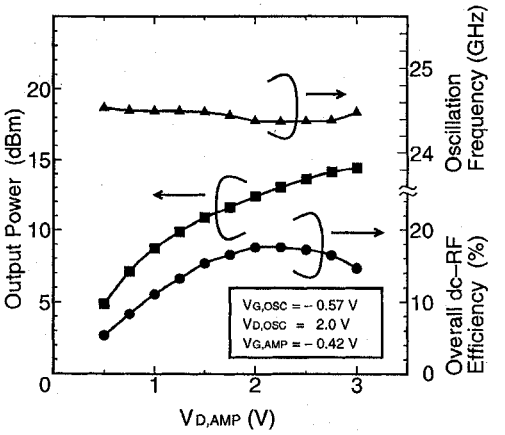

Fig. 10. Output power, oscillation frequency, and overall dc-RF efficiency as a function of amplifier drain voltage ($V_{D,\mathrm{AMP}}$).

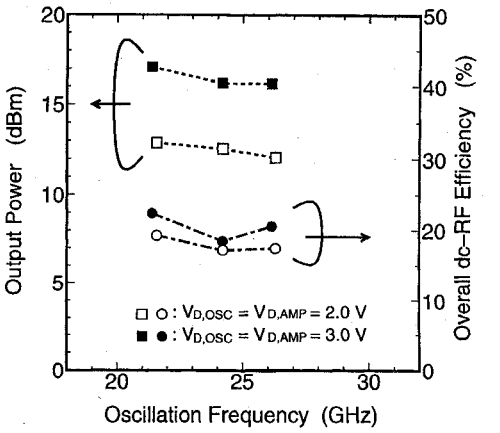

Fig. 11. Maximum output power and overall dc-RF efficiency for each oscillator at $V_{D,\mathrm{OSC}} = V_{D,\mathrm{AMP}} = 2.0$ V and $V_{D,\mathrm{OSC}} = V_{D,\mathrm{AMP}} = 3.0$ V.

was higher than 16 dBm. The 21 GHz oscillator output power was 17 dBm with an overall dc-RF efficiency of 22% at $V_{D,\mathrm{OSC}} = V_{D,\mathrm{AMP}} = 3.0$ V.

V. Conclusion

The design approach, fabrication process, and performance of a K-band MMIC oscillator incorporating a buffer amplifier on a single chip were described. The optimum load line for the oscillator was chosen in order to have an oscillation frequency insensitive to the effect of the subsequently connected amplifier based on the device-circuit interaction concept. By changing the length of the source feedback line, the oscillation frequency was varied from 21 GHz to 26 GHz. For all cases, the output power was higher than 16dBm. At 21 GHz, the output power of the oscillator recorded 17 dBm with an overall dc-RF efficiency of 22%.

The output power of the developed MMIC oscillators is sufficiently high to directly drive mixers in transmitter/receiver modules with no additional power amplification.

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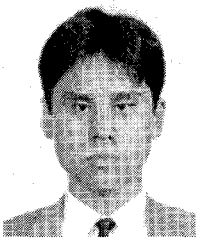

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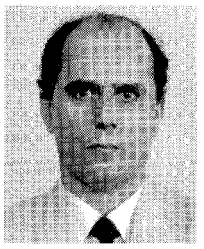

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